WEST Search History

DATE: Monday, May 20, 2002

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L9	(determin$3 or calculat$3 or comput$3 or charg$3) fee (information or document or content or record or data or file)	68	L9
L8	l7 and (determin$3 or calculat$3 or comput$3 or charg$3) fee	9	L8
L7	(provi$3 or present$6 or transmit$5 or transfer$3 or send$3) near5 (information or document or content) near7 (mail or email) near5 address	953	L7
L6	('20020048449')[ABPN1,NRPN,PN,TBAN,WKU]	1	L6
L5	fee address$3	15	L5
L4	fee near5 address$3	144	L4
L3	charg$3 near5 (fee or money) and (information or document or content) near7 (mail or email) near5 address near5 (provi$3 or present$6 or transmit$5 or transfer$3 or send$3)	47	L3
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L2	(determin$6 or comput$4 or calculat$3) near5 (fee or pay$3 or money) and (information or document) near7 (mail or email) near5 address	108	L2
DB=USPT; PLUR=YES; OP=ADJ			
L1	(determin$6 or comput$4 or calculat$3) near5 (fee or pay$3 or money) and (information or document) near7 (mail or email) near5 address	76	L1

END OF SEARCH HISTORY

```
 Set  Items  Description
      ---  -----  -----------
?ecs fee

Ref   Items  Index-term
E1   136189  CS
E2        1  CS AND M
E3        0 *CS FEE
E4        1  CS GROUP INC. SPECIAL EFFECTS DIV.
E5        1  CS&L III
E6        1  CS-045 (DRUG)
E7        1  CS-2 (ARTIFICAL SATELLITE)
E8        1  CS-3 (ARTIFICIAL SATELLITE)
E9    27346  CSA
E10       1  CSA INTERNATIONAL
E11     746  CSAA
E12       2  CSAAA

          Enter P or PAGE for more
?exs fee
>>>Temporarily unable to access SearchSaves
?ecs tdfee

Ref   Items  Index-term
E1        1  CS AND M
E2        1  CS GROUP INC. SPECIAL EFFECTS DIV.
E3        0 *CS TDFEE
E4        1  CS&L III
E5        1  CS-045 (DRUG)
E6        1  CS-2 (ARTIFICAL SATELLITE)
E7        1  CS-3 (ARTIFICIAL SATELLITE)
E8    27346  CSA
E9        1  CSA INTERNATIONAL
E10     746  CSAA
E11       2  CSAAA
E12       2  CSAAC

          Enter P or PAGE for more
?exs tdfee
>>>SET HILIGHT: use ON, OFF, or 1-5 characters
Processed  10 of  21 files ...
Processing
Completed processing all files
        15709628  INFORMATION
         8128754  DATA
          981763  DOCUMENT
            2464  ASYNCHRONOUSLY
         3043561  ADDRESS?
      S1      63  (INFORMATION OR DATA OR DOCUMENT) (S) ASYNCHRONOUSLY (S)
                  ADDRESS?
              63  S1
         2635258  COLLECT?
         1328981  PAYMENT
         1023625  FEE
           32273  COLLECT?(5N)(PAYMENT OR FEE)
      S2       0  S1 AND COLLECT? (5N) (PAYMENT OR FEE)
              63  S1
         1328981  PAYMENT
         1023625  FEE
      S3       2  S1 AND (PAYMENT OR FEE)
?t s1/med, k/all
>>>"MED" is not a valid format name in file(s): 9, 15-16, 18, 20, 148, 160,
   267-268, 473, 475, 481, 485, 583, 621, 623-626, 635, 636
?t s1/medium, k/all

 1/K/1     (Item 1 from file: 15)
DIALOG(R)File  15:ABI/Inform(R)
```

01741189 03-92179
Improving the WWW: Caching or multicast?
Rodriguez, Pablo; Ross, Keith W; Biersack, Ernst W
Computer Networks & ISDN Systems v30n22,23 PP: 2223-2243 Nov 25, 1998
ISSN: 0376-5075 JRNL CODE: CNI

...ABSTRACT: popular Web documents are considered. In the first scheme the sender repeatedly transmits the Web **document** into a multicast **address** , and receivers **asynchronously** join the corresponding multicast tree to receive a copy. In the 2nd scheme, the **document** is distributed to the receivers through a hierarchy of Web caches. Analytical models for both...

... latency, saves network bandwidth, and reduces the load on the origin server. Furthermore, if a **document** is updated randomly rather than periodically, the relative performance of CMP improves. Therefore, the best ...

1/K/2 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00621997 92-37099
Client-Server Computing
Sinha, Alok
Communications of the ACM v35n7 PP: 77-98 Jul 1992
ISSN: 0001-0782 JRNL CODE: ACM
WORD COUNT: 11708

...TEXT: on DOS, Windows, OS/2, and Unix platforms.

Applications interact with NetBIOS support through a **data** structure called Network Control Block (NCB) (see Figure 4); (Figure 4 omitted) An application mustan application can can function INT 5C with the **address** of NCB in register pair ES:BX to "submit" a NCB; in the OS/2...

...Return Code field of NCB. Almost all NCB commands can be executed either synchronously or **asynchronously** .

NetBIOS provides two kinds of data transfer methods--session support and datagram support. Session support...

1/K/3 (Item 3 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00616601 92-31703
X.400 Lite Provides Aid to LAN Users
O'Brien, Timothy
Network World v9n20 PP: 31, 34 May 18, 1992
ISSN: 0887-7661 JRNL CODE: NWW
WORD COUNT: 444

...ABSTRACT: LAN) users to implement X.400 messaging. X.400 allows LAN users to send messages **asynchronously** over dial-up lines instead of over more expensive communications links. Designed to work with...

... an international X.400 standards-compliant messaging system that utilizes a set of rules-based **address** management and routing features. The product includes software for client workstations and code for a...

... new product is a set of tools called ISOMAIL 400 that support the development of **document** transfer applications from both DOS and Microsoft Windows environments.

1/K/4 (Item 4 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00484477 90-10234
Memory Contention Bottleneck Eased in Terminals with VRAMs
Nesin, Richard; Li, Tak-Po
Computer Technology Review v9n16 PP: 89-92 Winter 1989
ISSN: 0278-9647 JRNL CODE: CTN

ABSTRACT: Dual-ported dynamic random access memory (VRAM) chips were developed to **address** the computer terminal design problem of memory contention, which occurs when 2 or more independent...

... and workstation design technology, generally have 2 ports that can, for the most part, operate **asynchronously** . Most allow the **data** transfer operation to be synchronized so a shift register can be loaded from a RAM array while **data** are being shifted out of the serial port. The CRT97C11 VIEW chip, which allows **addresses** to be manipulated in both horizontal and vertical dimensions, allows the VIEW to generate hardware...

... vertical window beginning and end coordinates via VIEW adds a 2nd dimension of flexibility to **data** placement on the screen. ...

1/K/5 (Item 5 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00227025 84-05586
SNA Distribution Services
Housel, Barron C.; Scopinich, Carol J.
IBM Systems Journal v22n4 PP: 319-343 1983
ISSN: 0018-8670 JRNL CODE: ISY

...ABSTRACT: Business Machines Corp. (IBM) Systems Network Architecture Distribution Services (SNADS). Previously, SNA focused on synchronous **data** distribution. However, along with the advent of office systems and other distributed applications has developed the need to provide a common architecture for the interchange of **data** **asynchronously** among diverse products and systems. SNADA offers a general asynchronous (delayed delivery) **data** distribution facility for SNA applications. The first implementations are for office systems applications. The review **addresses** : 1. objectives of an asynchronous **data** distribution service, 2. key architectural concepts, 3. the relationship between SNADS and the SNA synchronous...

1/K/6 (Item 6 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00012771 74-01393
SELECTION POINTERS FOR VOICE-BAND UNITS
DATA COMMUNICATIONS USER V3 N1 PP: 46-48 JAN 1974
ISSN: 0045-9682 JRNL CODE: DCU

...ABSTRACT: FULL-DUPLEX MODE WITH SERIAL OR PARALLEL FORMAT AND WHAT THE OPERATING SPEED AND EFFECTIVE **DATA** THROUGHPUT WILL BE. FOR HELP IN DECIDING WHICH VOICE- BAND MODEM OR COUPLER TO LEASE...

... THE SELECTION AND BUYER'S GUIDES, WHERE YOU WILL FIND COMPARISON CRITERIA AND THE NAMES, **ADDRESSES** AND TELEPHONE NUMBERS OF SUPPLIERS OF INDEPENDENT, OR NON-BELL MODEMS AND COUPLERS. DIAL-UP LINKS ARE HALF-DUPLEX LINES AND HAVE A MAXIMUM TRANSMISSION RATE OF ABOUT 2000 BPS

ASYNCHRONOUSLY AND 4[redacted] BPS SYNCHRONOUSLY, THOUGH [redacted]ME USERS HAVE OPERATED SUCCESSFULLY UP TO 7200 BPS. IF YOU NEED TO SEND **DATA** TO MANY DIFFERENT POINTS, THEN YOU WILL HAVE TO USE DIAL-UP LINES. OTHERWISE, IT MAY PAY TO INVESTIGATE THE USE OF LEASED LINES FOR YOUR **DATA** TRANSMISSION NEEDS.

1/K/7 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

07668834 Supplier Number: 63643231 (USE FORMAT 7 FOR FULLTEXT)
Afaria Wins, but the Competition Is Close -- Mobile Automation 2000 and Orbiter packages provide solid ease of use, but scalability and administration prove to be the difference for XcelleNet's Afaria. (Software Review) (Evaluation)
Hoffman, Richard
Network Computing, p66
July 24, 2000
Language: English Record Type: Fulltext
Article Type: Evaluation
Document Type: Magazine/Journal; Trade
Word Count: 4508

... provides a granular set of controls that lets you determine what kinds of files and **data** should be sent, depending on network connection type and speed (letting, for instance, certain large...

...s no autodiscovery feature. If the TCP port isn't available, Orbiter can send its **data** **asynchronously** using Microsoft Exchange/Outlook, Lotus cc:Mail or Lotus Notes. Each client must have a unique e-mail **address** to keep the queues distinct, and the Orbiter server must reside on a machine separate...

1/K/8 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

07459655 Supplier Number: 62711028 (USE FORMAT 7 FOR FULLTEXT)
Application Integration: Piecing E-Businesses Together. (Technology Information)
Seltzer, Larry J.
PC Magazine, p185
July 1, 2000
Language: English Record Type: Fulltext Abstract
Document Type: Magazine/Journal; General Trade
Word Count: 1030

... concept of e-business. Most vendors have settled on a few technologies and standards that **address** various aspects of integration, primarily in the area of communications between applications. A sampling would include XML as a **data** -interchange format, Enterprise Java Beans as a server architecture, CORBA and DCOM as programmatic methods for processes to call each other, message- queuing systems to let systems communicate **asynchronously** , and transaction monitors to ensure that operations complete properly.
A typical eai system will offer...

1/K/9 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06093671 Supplier Number: 53638381 (USE FORMAT 7 FOR FULLTEXT)
Architecture eyes latency, parallel issues. (Motorola's G4 microprocessor) (Product Announcement)

Fuller, Sam
Electronic Engineering Times, p82(1)
Jan 25, 1999
Language: English Record Type: Fulltext
Article Type: Product Announcement
Document Type: Magazine/Journal; Trade
Word Count: 983

... for each preload instruction.
In contrast, the DST instruction refers to a whole block of **data** described with a starting **address** , a block size (up to thirty-two 16-byte vectors), a number of blocks (1...

...to +32,768). DST effectively kicks off a direct-memory-access-controller operation that will **asynchronously** , and independently of the processor's instruction execution, bring **data** into the on-chip cache hierarchy.
The G4 processor supports up to four independent streams...

1/K/10 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

05187320 Supplier Number: 47915837 (USE FORMAT 7 FOR FULLTEXT)
TIBCO BELIEVES PUSH-BASED MESSAGING WILL PULL BUSINESS AWAY FROM ITS RIVALS
Computergram International, n3227, pN/A
August 18, 1997
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 255

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...inefficient use of bandwidth, especially in high-volume applications environments such as Web servers and **data** warehouses. Tibco says TIB/Rendezvous pushes message to servers **asynchronously** and ensures each request is only handled once, by using a server-based scheduler to...

...respective Internetprotocol (IP) multicasting technologies to create a single specification for reliable multicasting - including subject **addressing** - they will submit for standardisation to the Internet Engineering Task Force some time next year...

1/K/11 (Item 5 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04713356 Supplier Number: 46939770 (USE FORMAT 7 FOR FULLTEXT)
Slave PCI interface lowers the cost of ISA conversion
Electronic Engineering Times, pP16
Dec 2, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 165

The device interfaces adapter control, **address** and **data** lines to a host computer's MPU and memory architecture at 33-MHz PCI speeds...

...big-endian systems is performed directly in the interface chip's logic. Five local-bus **address** spaces and four chip selects are included, as is a bidirectional FIFO to provide zero...

...support muxed and non-muxed 8-, 16- or 32-bit local buses, which can run **asynchronously** to the PCI clock.
In a 160-pin plastic quad flat pack, the PCI9050 is...

1/K/12 (Item 6 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02952181 Supplier Number: 43994677 (USE FORMAT 7 FOR FULLTEXT)
JAPAN's CHIP CONTENDERS FOR DIGITAL ASSISTANT MARKET - 2: HITACHI's FULL-FEATURED ENTRY
Computergram International, n2220, pN/A
July 28, 1993
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 1315

... chip solution. Both chips include a 32-bit RISC-based CPU and a 32-bit **address** bus. Although they hobble along on a 16-bit external bus, there is a 22-bit unmultiplexed **data** bus for designers that want to **address** up to 4Gb of RAM. The chips run at either 5V or 3.3V in...

...of them externally. Also included are two serial ports which can be programmed synchronously or **asynchronously** at baud rates decided by the chip's internal clock - up to 5M-bits per...

1/K/13 (Item 7 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

01569945 Supplier Number: 41925169 (USE FORMAT 7 FOR FULLTEXT)
SRAMs race for 10 ns
Electronic Engineering Times, p110
March 11, 1991
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1212

... cache controller will not know at the beginning of a write cycle whether or not **data** is actually to be written into the **data** SRAMs. If there is a cache hit, the cycle should go ahead. But if there is a cache miss-- **information** that won't come along until near the end of the cycle--the write must be aborted, to prevent overwriting some innocent line of **data** . Motorola designers have **addressed** this sticky issue by providing a late-write abort signal. The abort strobe can arrive **asynchronously** , even late in the write cycle, to prevent the write from finishing.
It is just...

1/K/14 (Item 1 from file: 18)
DIALOG(R)File 18:Gale Group F&S Index(R)

01107073 Supplier Number: 40675271
Racal-Vadic readies V.32 modem
PC Week, pC22
Feb 6, 1989
ISSN: 0740-1604
Language: English Record Type: Abstract
Document Type: Magazine/Journal; Tabloid; General Trade

ABSTRACT:
Racal-Vadic is introducing the 9632VP 9,600 bps full-feature modem to **address** the corporate desktop computer market. The 9632VP is fully compatible with most lower speed modems, can operate over dial-up or leased lines synchronously or **asynchronously** , and can generate transmission speeds up to 19.2 Kbps using the MNP Class 5 **data** -compression method. The unit also offers Microcom Networking Protocol Class 2-4 error control, a...

1/K/15 (Item 2 from file: 18)
DIALOG(R)File 18:Gale Group F&S Index(R)

01042777 Supplier Number: 40525794
Single board logic analyser for VME bus-based systems
Electronic Engineering, p69
Oct, 1988
ISSN: 0013-4902
Language: English Record Type: Abstract
Document Type: Magazine/Journal; Trade

ABSTRACT:
...come in two sorts, the timing analysers which have few input channels and are sampled **asynchronously** at high speeds, and state analysers which have a large number of input channels and...

...systems. A 32 bit VME-bus system requires a logic analyser that is capable of **data** collection on 90 channels or more simultaneously and at speed of 10 MHz. This is...

...for statistical and performance analysis software for the VME systems which will provide histograms for **address** distribution, interrupt activity and bus master levels.
...

1/K/16 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

11971681 SUPPLIER NUMBER: 61353404 (USE FORMAT 7 OR 9 FOR FULL TEXT)
GUEST VIEWPOINT:A CRITICAL LOOK AT IA-64 -- Massive Resources, Massive ILP, But Can It Deliver?(Technology Information)(Editorial)
Hopkins, Martin
Microprocessor Report, 14, 2, NA
Feb, 2000
DOCUMENT TYPE: Editorial ISSN: 0899-9341 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 3882 LINE COUNT: 00305

... well as instructions to modify, test, and retrieve NaT values. Moving loads ahead of stores (**data** speculation) requires a memory-alias-detection table-in IA-64 this hardware table is called the advanced-load- **address** table, or ALAT. Special loads place entries in the ALAT, and stores whose **addresses** match an ALAT entry will remove that entry. For **data** speculation, check instructions access the ALAT to detect stores to a memory location that has been fetched by a load that was moved ahead of the store. (**Data** speculation can use a check load that does the recovery in some simple cases.) The...

...stack-frame overflow might occur at a frequent call point, a register stack engine (RSE) **asynchronously** saves and restores registers in the background. This RSE mechanism must take page faults, etc...

1/K/17 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

11501175 SUPPLIER NUMBER: 57588385 (USE FORMAT 7 OR 9 FOR FULL TEXT)
PATENT WATCH.(News Briefs)
Belgard, Rich
Microprocessor Report, 13, 15, NA
Nov 15, 1999

ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 682 LINE COUNT: 00061

... processor.
The claims include a function unit that contains at least a function register, a **data** register, a result **address** register and a monitoring circuit. When the function, **data** and **address** registers have been loaded, as detected by the monitoring circuit, the function unit may begin its operation, **asynchronously** .
5,903,750
Dynamic branch prediction for branch instructions with multiple targets
Filed: November 20...

1/K/18 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

11484886 SUPPLIER NUMBER: 56950204 (USE FORMAT 7 OR 9 FOR FULL TEXT)
80186. (Brief Article)
EDN, 44, 19, 122
Sept 16, 1999
DOCUMENT TYPE: Brief Article ISSN: 0012-7515 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 530 LINE COUNT: 00046

The core architecture includes the processor-execution and the bus-interface units, which **asynchronously** communicate to the outside world via an 8-or a 16-bit multiplexed system bus. Some AMD 186s support a nonmultiplexed **address** / **data** bus, which frees the processor to run at nearly twice the speed of standard 80C186...

1/K/19 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

10769343 SUPPLIER NUMBER: 53638381 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Architecture eyes latency, parallel issues. (Motorola's G4 microprocessor) (Product Announcement)
Fuller, Sam
Electronic Engineering Times, 82(1)
Jan 25, 1999
DOCUMENT TYPE: Product Announcement ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1096 LINE COUNT: 00094

... for each preload instruction.
In contrast, the DST instruction refers to a whole block of **data** described with a starting **address** , a block size (up to thirty-two 16-byte vectors), a number of blocks (1...

...to +32,768). DST effectively kicks off a direct-memory-access-controller operation that will **asynchronously** , and independently of the processor's instruction execution, bring **data** into the on-chip cache hierarchy.
The G4 processor supports up to four independent streams...

1/K/20 (Item 5 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09894097 SUPPLIER NUMBER: 20028560 (USE FORMAT 7 OR 9 FOR FULL TEXT)
16 bit. (EDN's 24th annual microprocessor/microcontroller directory on 16-bit devices) (Cover Story) (Directory)
Levy, Markus

EDN, v42, n20, p80(12)
Sep 25, 1997
DOCUMENT TYPE: Cover Story Directory ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 7645 LINE COUNT: 00607

... data segments.
The core architecture includes the processor-execution and the bus-interface units, which **asynchronously** communicate to the outside world via an 8- or a 16-bit multiplexed system bus. Some AMD 186s support a nonmultiplexed **address / data** bus, which frees the processor to run at nearly twice the speed of standard 80C186...

1/K/21 (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09459774 SUPPLIER NUMBER: 19370523 (USE FORMAT 7 OR 9 FOR FULL TEXT)
High-speed DRAMs keep pace with high-speed systems. (dynamic random access memory)
Hampel, Craig
EDN, v42, n3, p141(5)
Feb 3, 1997
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2623 LINE COUNT: 00206

... is a page-mode DRAM with the addition of a register set that holds the **data** output. This feature allows the core to access the next column **address** sooner, resulting in a 30% speed improvement over comparable page-mode DRAMs. The controller presents row- **address** strobes (RASs) and column- **address** strobes (CASs) to the core, **asynchronously** to the bus clock. EDO DRAMs use a single bank architecture and, therefore, must process...

1/K/22 (Item 7 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09020116 SUPPLIER NUMBER: 18754207 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Use add/pass-shift multipliers for FPGA-based FIR filters. (field-programmable gate array; finite-impulse-response)(includes related article on programmable function units)
Stuby, Rick
Electronic Design, v44, n18, p85(6)
Sep 3, 1996
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 3305 LINE COUNT: 00253

... precalculated for all possible factors and stored in ROM. The factors then are used as **addressing** into the ROM. The product is read back as **data** from the ROM. Figure 2 is a diagram of a 8x8 ROM multiplier. ROM multipliers are commonly implemented in FPGAs and operate synchronously and **asynchronously** .
It should be noted, however, that ROM-based designs become intractable when large factors are...

1/K/23 (Item 8 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08995630 SUPPLIER NUMBER: 18731287 (USE FORMAT 7 OR 9 FOR FULL TEXT)
MESSAGE-ORIENTED MIDDLEWARE ASSOCIATION, COOL TO IBM's MQSERIES OFFER, IS STILL SEEKING COMMON MESSAGING GROUND.
Computergram International, n3009, pCGN09300013

Sep 30, 1996
ISSN: 0268-716X LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 520 LINE COUNT: 00046

TEXT:
...by processes running on distributed systems. A process running on one system can instruct or **address** a process on another system over a network **asynchronously** , and unlike remote procedure calls, which literally invoke remote procedures onto the local system, transmits...

...a database management system or an operating system. In heterogeneous environments, clients have to exchange **information** across networks using multiple communications protocols and operating systems environments. Candle vice-president of solutions...

1/K/24 (Item 9 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2002 The Gale Group. All rts. reserv.

08664642 SUPPLIER NUMBER: 18251692 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Painting success stories with numbers.(Feature Report: Financial Management)
Bohdanowicz, Richard
Computer Dealer News, v12, n5, p26(2)
March 7, 1996
ISSN: 1184-2369 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 795 LINE COUNT: 00070

... of Technology, Kempthorne has undertaken research projects sponsored by the International Financial Services Research Center **addressing** statistical modelling problems in risk management. One problem concerns the modelling of global portfolio risks with asynchronous prices from multiple sources. Daily price **data** for multinational securities are observed **asynchronously** and can be unavailable due to the holidays or market closes which vary across the...

1/K/25 (Item 10 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2002 The Gale Group. All rts. reserv.

07952883 SUPPLIER NUMBER: 17148434 (USE FORMAT 7 OR 9 FOR FULL TEXT)
MESSAGE-ORINETED MIDDLEWARE BODY IS "YEARS AWAY" FROM GOAL OF INTEROPERABLE MESSAGING MIDDLEWARE.
Computergram International, pCGN06270012
June 27, 1995
ISSN: 0268-716X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 435 LINE COUNT: 00039

TEXT:
...seeking a standard that will govern messaging software. Introducing its white paper, Building Your Enterprise **Information** Infrastructure With Message Oriented Middleware, the Association, which has stolen MOMA, the acronym by which...

...also director of strategic alliances at PeerLogic Inc, said this kind of problem will be **addressed** by the market over time and said the association's task is only to "educate...

...processes running on distributed systems. It enables a process on one system to instruct or **address** a process on another system over a network **asynchronously** , and - unlike remote procedure calls which invoke remote procedures onto the local system - transmits multiple...

...a database management system or an operating system. In heterogeneous environments clients have to exchange **information** with database servers

across a network, using different communications protocols and operating systems. "MQSeries and message-oriented middleware in general is in the business of getting this **information** across," said Steve Craggs, business manager of IBM Corp's MQSeries messaging software based in...

1/K/26 (Item 11 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

07667995 SUPPLIER NUMBER: 16565121 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DRAM king ousted. (synchronous dynamic random access memory)
Parry, Simon
Electronics Weekly, n1708, p16(1)
Jan 25, 1995
ISSN: 0013-5224 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1265 LINE COUNT: 00100

... system clock operating up to 100MHz. This contrasts with traditional DRAM technology which is controlled **asynchronously** ; the processor despatches a set of **addresses** and waits, while the DRAM performs several internal functions such as activating the word and bit lines, until the **data** is returned. Conversely under synchronous control of the system clock, the **addresses** are latched in the DRAM until the device is ready to deliver the **data** after a preprogrammed number of clock cycles, During this time the processor can perform other...

1/K/27 (Item 12 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

07246821 SUPPLIER NUMBER: 15321238 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Quantify critical-timing risks with statistical analysis. (includes a related article on a worst-case circuit analysis) (Tutorial)
Vorgert, James J.
EDN, v39, n4, p95(6)
Feb 17, 1994
DOCUMENT TYPE: Tutorial ISSN: 0012-7515 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4733 LINE COUNT: 00382

... A(0:16) and CS(0:3) outputs. From there, the signals travel to the **address** and control inputs of the ROM devices. The path **asynchronously** propagates through one of the ROMs and drives the inputs of a standard bus-interface device. The buffer interface in turn drives the microprocessor's **data** input (CPU).

Individual paths include many permutations of the same basic structure, which is a...

1/K/28 (Item 13 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

06808376 SUPPLIER NUMBER: 14832081 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Let's get synchronous. (synchronous dynamic random access memory)
Parry, Simon
Electronics Weekly, n1662, p16(1)
Dec 1, 1993
ISSN: 0013-5224 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 902 LINE COUNT: 00069

... system clock operating up to 100MHz. This contrasts with traditional DRAM technology which is controlled **asynchronously** ; the processor despatches a set of **addresses** and waits, while the DRAM performs several internal functions such as activating the word and bit

lines, until the **data** [redacted] returned. Conversely under synchronous control of the system clock, the **addresses** are latched in the DRAM until the device is ready to deliver the **data** after a preprogrammed number of clock cycles. During this time the processor can perform other...

1/K/29 (Item 14 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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06680073 SUPPLIER NUMBER: 14206276 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Japan's chip contenders for digital assistant market - 2: Hitachi's full-featured entry. (Hitach SH7032 and SH7034)
Bradbury, Danny
Computergram International, CGI07280006
July 28, 1993
ISSN: 0268-716X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1410 LINE COUNT: 00107

... chip solution. Both chips include a 32-bit RISC-based CPU and a 32-bit **address** bus. Although they hobble along on a 16-bit external bus, there is a 22-bit unmultiplexed **data** bus for designers that want to **address** up to 4Gb of RAM. The chips run at either 5V or 3.3V in...

...of them externally. Also included are two serial ports which can be programmed synchronously or **asynchronously** at baud rates decided by the chip's internal clock - up to 5M-bits per...

1/K/30 (Item 15 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2002 The Gale Group. All rts. reserv.

06091676 SUPPLIER NUMBER: 12344608 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Futurebus+ offers innovative protocols; silicon support emerging from three vendors.
Theus, John
Microprocessor Report, v6, n9, p16(4)
July 8, 1992
ISSN: 0899-9341 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 3066 LINE COUNT: 00240

... during a single transaction. The main restriction is that packets must occupy an ascending contiguous **address** space. When a packet transfer is started, the compelled **data** handshake signals are used for controlling the request and approved/denied protocol for the subsequent packets. This protocol runs **asynchronously** with respect to the packet transfer and is allowed to run ahead so it can...

...send. This multiple-packet-mode protocol can be used for both cached and non-cached **data** .
Hierarchical Cache Coherency
When the parallel protocols for Futurebus were being designed in the mid...

1/K/31 (Item 16 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2002 The Gale Group. All rts. reserv.

05808052 SUPPLIER NUMBER: 11983917 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Synchronous cache RAMs run at 50 MHz. (random access memory) (Cypress Semiconductor Corp.'s CY7B173 and CY7B174 semiconductor memory) (Hardware Review) (Evaluation)
Quinnell, Richard A.
EDN, v37, n1, p73(1)
Jan 2, 1992

DOCUMENT TYPE: Evaluation ISSN: 0012-7515 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 396 LINE COUNT: 00030

Both memories are organized as 32k x 9 bits. They operate synchronously, sampling the **address** , **data** , and control lines on the rising edge of the clock input signal. The clock's...

...time is 20 nsec, allowing operation at 50 MHz. Only the output-enable line operates **asynchronously** , setting the **data** output lines to high impedance within 7 nsec of de-assertion.
For the memories to...

1/K/32 (Item 17 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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05735488 SUPPLIER NUMBER: 12201318
X.400 Lite provides aid to LAN users. (International Standards Open Communications Resources to simplify implementation of X.400 messaging services) (Product Announcement)
O'Brien, Timothy
Network World, v9, n20, p31(2)
May 18, 1992
DOCUMENT TYPE: Product Announcement ISSN: 0887-7661 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

ABSTRACT: International Standards Open Communications Resources (ISOCOR), a **data** -communications startup firm, introduces X.400 Lite, a new local-area-network software product that lets users send X.400 messages **asynchronously** over dial-up lines instead of costly dedicated communications links. X.400 Lite is designed...

...any microcomputer application and is an international standards-compliant messaging system that uses rules-based **address** management and routing features. It includes software for client workstations and code for a communications...

1/K/33 (Item 18 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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04606390 SUPPLIER NUMBER: 08615390 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Floating-point chips boost (microprocessor) performance. (includes a related article on the ANSI/IEEE STD 754-1985 for Binary Floating-Point Arithmetic)
Gallant, John; Travis, Bill
EDN, v35, n12, p63(6)
June 7, 1990
ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2526 LINE COUNT: 00202

... Error signal that signifies the occurrence of an exception.
The main processor uses the A31 **address** line and the M/IO line to designate the coprocessor as a peripheral in a reserved area of the upper I/O **address** space. All memory transfers to and from the coprocessor pass through the main processor using...

...pipelined or nonpipelined bus cycles. The coprocessor can run synchronously with the CPU clock or **asynchronously** by using a separate clock. The processor-coprocessor handshake allows concurrent processing. When writing exception handlers, be careful to prevent the main processor from using erroneous **data** if an exception occurs. Prices for the 80387 DX range from $284.75 for the...

1/K/34 (Item 19 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

04530762 SUPPLIER NUMBER: 08216588 (USE FORMAT 7 OR 9 FOR FULL TEXT)
C&T unveils multiprocessor chip set; M/PAX design uses 128-bit bus, directory-based cache coherency. (Chips and Technologies' Multi-Processor Architecture eXtension CS9239 chip set) (product announcement)
Microprocessor Report, v4, n3, p1(3)
Feb 21, 1990
DOCUMENT TYPE: product announcement ISSN: 0899-9341 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1850 LINE COUNT: 00142

... multiprocessor interconnect bus is quite unlike conventional system buses. In addition to the 128-bit **data** path, there is a 32-bit **address** bus and 24 control signals. All transfers are synchronous to the bus clock, which is...

...12.5 to 25 MHz. The modest clock rate minimizes switching noise, while the wide **data** path provides high bandwidth. The processor/cache modules can operate **asynchronously** to the bus for maximum flexibility in selecting clock rates. They can also operate synchronously...

1/K/35 (Item 20 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

04158434 SUPPLIER NUMBER: 07993504 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Speed memory, ease timing requirements with VRAM functions. (video random-access memory chips)
Mailloux, Jeff; Mills, Jeffrey; Seibert, Michael J.
Electronic Design, v37, n24, p95(5)
Nov 23, 1989
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2439 LINE COUNT: 00184

... applications.
Besides having two I/O ports, the video RAM also sports very wide internal **data** paths between the dynamic RAM and the serial-access memory. For a 256k-by-4 bit VRAM, **data** I/O and internal **data** transfer are done using three separate bidirectional **data** paths: the four-bit random access I/O port, the four internal 512-bit wide...

...I/O port for the SAM. Each of the I/O ports may be operated **asynchronously** and independently of the other, except when **data** is transferred internally between them. The rest of the VRAM's circuitry consists of the control, timing, and **address** -decoding logic.
SPECIAL FUNCTIONS
The Joint Electron Device Engineering Council (Jedec) established two standards: one...

1/K/36 (Item 21 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

04101422 SUPPLIER NUMBER: 07586094 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Lab notes. (high-speed communications in DOS and OS/2) (part 1 of 2)
Prosise, Jeff
PC Magazine, v8, n16, p307(8)
Sept 26, 1989
ISSN: 0888-8507 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4309 LINE COUNT: 00329

... hardware interrup[redacted] of equal and lower priority a[redacted] withheld from the CPU.

READ-COM operates **asynchronously** from the main body of the program, which is contained in the procedure TERM. TERM executes a simple loop, alternately polling the keyboard and serial input buffers for **data** . When a keycode appears in the keyboard buffer, it is read, displayed, and transmited; when...

...displayed. The queue is checked for new characters simply by comparing die head and tail **addresses** . If the **addresses** are the same, no **data** is waiting to be read.

Characters are read from the queue with the subroutine READ...

1/K/37 (Item 22 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03932595 SUPPLIER NUMBER: 07440038 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Four times as good. (Hardware Review) (Hayes V-series Smartmodem 9600 plus Quad) (evaluation)
Collin, Simon
PC User, n108, p83(2)
June 7, 1989
DOCUMENT TYPE: evaluation ISSN: 0263-5720 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1657 LINE COUNT: 00123

... an X.25 cloud. These are a normal modem attached to the PC which sends **data** **asynchronously** to a receiving modem, which is attached to a PAD (packet assembler/disassembler) that correctly labels the **data** with the destination and source **addresses** , and sorts them into packets, which are then sent across the network.

The advantage of...

1/K/38 (Item 23 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03715217 SUPPLIER NUMBER: 06814996 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Configurable chip eases control-system design.
Bursky, Dave
Electronic Design, v36, n24, p63(5)
Oct 27, 1988
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1878 LINE COUNT: 00143

... file or to an external device.

An eight-word FIFO register lets a host microprocessor **asynchronously** load commands or **data** into the controller. The 22-bit word length in the FIFO register is employed, so that if **data** values are to be loaded into the register file, the lower 16 bits of the 22-bit word sent over the host **data** bus represent the **data** , and the next five bits--the lower five bits of the host-interface **address** bus--represent the register location into which the **data** will be loaded (R0 to R31). The sixth bit of the host-interface **address** bus signifies whether the word loaded into the FIFO register is a command or **data** word. If it's a command, the lower 10 bits of the host- **data** bus are used as a branch **address** to one of the 1024 memory locations in the EPROM.

The 10-bit sequencer addresses...

1/K/39 (Item 24 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03523489 SUPPLIER NUMBER: 06762075 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Roll your own test system with PC XT, AT plug-in modules.
Milne, Bob
Electronic Design, v36, n10, p47(3)
April 28, 1988
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1359 LINE COUNT: 00106

... at companies building test systems for resale.
Bitwise Design's initial product, the Acquisition Module, **addresses** the response side of things, capturing **data** either synchronously or **asynchronously** , on 40 channels, at up to 25 MHz.
For synchronous sampling, three rising-edge and...

1/K/40 (Item 25 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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02825371 SUPPLIER NUMBER: 04244157 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Computers and digital electronics. (1986 Electrical and Industrial Electronics Reference Issue)
Machine Design, v58, p85(29)
May 15, 1986
ISSN: 0024-9114 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 9101 LINE COUNT: 00759

... to communication problems.
Most of these problems occur where several devices simultaneously try to send **information** over the system bus. Since many of the **data** , **address** , and control lines must be bidirectional, no two devices should attempt to pass signals on...

...prioritizing the devices which may control the system bus. In some systems where devices operate **asynchronously** (not all at the same speed), the bus must provide a format for handshaking or...

...signals between components. This synchronization might be required, for example, when a system memory delivers **data** faster than particular input/output devices can accept it.
There are a number of bus...

1/K/41 (Item 26 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2002 The Gale Group. All rts. reserv.

02486216 SUPPLIER NUMBER: 04015270 (USE FORMAT 7 OR 9 FOR FULL TEXT)
New power for board-level computers.
Bahniuk, Douglas
Machine Design, v57, p106(6)
Nov 7, 1985
ISSN: 0024-9114 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2492 LINE COUNT: 00195

... each employs to provide communication and control facilities.
Multibus: The original Mutibus uses 16-bit **data** transfer lines, although it also allows eight-bit transfers. **Data** transfers **asynchronously** -- transfers are not tried to a system clock. The bus uses what is called centralized...

...bus is not miltiplexed and contains lines that are dedicated to handling interrupts. Two separate **address** spaces are supported for memory and I/O. The bus allows the **addressing** of up to 16, bytes of memory and up to 64KI/P ports.
Mutibus II...

1/K/42 (Item 27 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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02333712 SUPPLIER NUMBER: 03789995 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Computers and electronic controls. (1985 Electrical & Electronics Reference Issue)
Machine Design, v57, p97(12)
May 30, 1985
ISSN: 0024-9114 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 7424 LINE COUNT: 00617

... to communication problems.
Most of these problems occur where several devices simultaneously try to send **information** over the system bus. Since many of the **data** , **address** , and control lines must be bidirectional, no two devices should attempt to pass signals on...

...prioritizing the devices which may control the system bus. In some systems where devices operate **asynchronously** (not all at the same speed), the bus must provide a format for handshaking or...

...signals between components. This synchronization might be required, for example, when a system memory delivers **data** faster than particular input/output devices can accept it.
There are a number of bus...

1/K/43 (Item 28 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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02031370 SUPPLIER NUMBER: 03285223 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Control and automation systems. (1984 Electrical & Electronics Reference Issue)
Machine Design, v56, p85(15)
May 31, 1984
ISSN: 0024-9114 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 9414 LINE COUNT: 00777

... to communication problems.
Most of these problems occur where several devices simultaneously try to send **information** over the system bus. Since many of the **data** , **address** , and control lines must be bidirectional, no two devices should attempt to pass signals on...

...prioritizing the devices which may control the system bus. In some systems where devices operate **asynchronously** (not all at the same speed), the bus must provide a format for handshaking or...

...signals between components. This synchronization might be required, for example, when a system memory delivers **data** faster than particular input/output devices can accept it.
Thee are a number of bus...

1/K/44 (Item 29 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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01752175 SUPPLIER NUMBER: 02767846 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Factory automation systems.
Machine Design, v55, p101(15)
May 19, 1983
ISSN: 0024-9114 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 11420 LINE COUNT: 00935

... to communication problems.
Most of these problems occur where several devices simultaneously try to send **information** over the system bus. Since many of the **data** , **address** , and control lines must be bidirectional, no two devices should attempt to pass signals on...

...prioritizing the devices which may control the system bus. In some systems where devices operate **asynchronously** (not all at the same speed), the bus must provide a format for handshaking or...

...signals between components. This synchronization might be required, for example, when a system memory delivers **data** faster than particular input/output devices can accept it.
There are a number of bus

1/K/45 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

02246956
IDT PREMIERES 25 ns FOUR PORT WITH 160 MEGABYTE PER SECOND BUS BANDWIDTH
News Release June 15, 1989 p. 1

... DSP) applications, including radar systems, local area networks (LANs) and graphics processors. Featuring independent asynchronous **address** , **data** and control lines, each port communicates via a standard SRAM interface that can access any location in memory simultaneously and **asynchronously** . This feature enables multiple controllers or processors to simultaneously access the same memory space, resulting...

1/K/46 (Item 2 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

02245153
An Industry First: Four-Port SRAMs From IDT
Semiconductor Industry & Business Survey July 10, 1989 p. N/A
ISSN: 0730-1014
FULL TEXT AVAILABLE IN FORMAT 7 OR 9 WORD COUNT: 230

... performance multiprocessing and DSP applications, including radar systems, LANs and graphics processors.
Featuring independent asynchronous **address** , **data** and control lines, each port communicates via a standard SRAM interface that can access any location in memory simultaneously and **asynchronously** . This feature enables multiple controllers or processors to simultaneously access the same memory space, resulting...

1/K/47 (Item 3 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

02119923
Racal-Vadic readies V.32 modem
PC Week February 6, 1989 p. C22
ISSN: 0740-1604

Racal-Vadic is introducing the 9632VP 9,600 bps full-feature modem to **address** the corporate desktop computer market. The 9632VP is fully compatible with most lower speed modems, can operate over dial-up or leased lines synchronously or **asynchronously** , and can generate transmission speeds up to 19.2 Kbps using the MNP Class 5 **data** -compression method. The unit also offers Microcom Networking Protocol Class 2-4 error control, a...

1/K/48 (Item 4 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

02093815
Single board logic analyser for VME bus-based systems
Electronic Engineering October, 1988 p. 69-72
ISSN: 0013-4902

... come in two sorts, the timing analysers which have few input channels and are sampled **asynchronously** at high speeds, and state analysers which have a large number of input channels and...

... systems. A 32 bit VME-bus system requires a logic analyser that is capable of **data** collection on 90 channels or more simultaneously and at speed of 10 MHz. This is...

... for statistical and performance analysis software for the VME systems which will provide histograms for **address** distribution, interrupt activity and bus master levels.
...

1/K/49 (Item 5 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

01375638
Fujitsu.
DEMPA DIGEST June 30, 1986 p. 5

... The MB8421 and MB8422 are suitable for serving as the common memory in a decentralized **data** processing system. It is possible with these SRAMs to access from the 2 boards, mutually independently and **asynchronously** , to any **address** of the memory. The random access memorys are designed to resolve such problems as the...

1/K/50 (Item 6 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

01063417
Says Memory Is Key in 32-Bit-MPU-Based Sys.
Electronic News July 9, 1984 p. 761

...places constraints on CPU designers to share the microprocessor bus. This concept involves storing key **data** in memory registers and in an MPU translation look-aside buffer rather than moving **data** across the bus for each use. The 32-bit-width bus in the 32032 microprocessor more efficiently accommodates **data** in workstation applications that are 32-bits in size. To further improve the bus efficiency of instruction fetching, accesses of instruction memory are made **asynchronously** to execution. With such a configuration, general-purpose registers in the CPU and in the...

... over the memory bus, while a cache of recently-used translations in the MMU allows **address** translation to proceed with infrequent access to the large memory-based translation tables.
...

1/K/51 (Item 7 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

01009235
Multiprocessing 32-bit buses are starting to blossom.
Electronics March 22, 1984 p. 24,1251

New 32-bit buses stress high bandwidths, sophisticated **addressing** schemes, and multiple pathways. For example, the VMEbus, recently upgraded with the expansion of VMXbus...

... 3 pathways while Multibus II features 5 busses. Both buses have full 32-bit primary **data** and **addressing** pads, but Multibus II uses multiplexing to achieve what VMEbus does with dedicated **addressing** and **data** links. While Multibus II uses a synchronous timing scheme and VME runs **asynchronously** , both achieve a 40+ Mbytes per second **data** transfer. The most important common attribute of these 2 buses is their open-system architecture...

1/K/52 (Item 8 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

00961784
Mostek's serial input/output (SIO) chip is the dual-channel, multiprotocol communications converter.
Electronic Engineering Times October 24, 1983 p. 56-641

...oriented protocols and synchronous bit-oriented protocols as well as having applications in such non- **data** uses as interfacing to cassette or floppy disc drivers. The MK68564 SIO, when used as a **data** communications device, transmits and receives serial **data** in a wide variety of communications protocols. When used as a microcomputer peripheral, it interacts with peripheral circuits, sharing the **data** , **address** , and control buses as well as being part of the 68000's interrupt structure. The ...

... in the full-duplex mode with each channel having program capability to operate synchronously or **asynchronously** . The SIO can be used for interfacing to peripherals such as hard-sectored floppy discs...

... IBM-compatible soft-sectored discs. The device also has an automatic feature to transmit CRC **data** when no other **data** are available for transmission. ...

1/K/53 (Item 9 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

00580552
Communications security with electronic mail is possible.
Office August, 1980 p. 22-26+1

Electronic Message Systems (EMS) allows users to **asynchronously** log-in, read, and respond to messages at their convenience. Provided the user carries a...

...his or her shoulder watching the preparation of the message. Encryption, implemented primarily with the **Data** Encryption Standard (DES) supported by the National Bureau of Standards, can be used to prevent active and passive wiretapping in EMS. The theoretical basis also exists for the concealment of **addresses** in EMS; this is not currently is use, however. CC Wood, management systems consultant, Computer Security Program, SRI International (Menlo Park, Calif), explains how messages and **addresses** can be concealed when using EMS.

1/K/54 (Item 1 from file: 267)

DIALOG(R)File 267:Finance Banking Newsletters

00002749
TECHNOLOGY CORNER
EFT REPORT
January 1, 1997 VOL: 20 ISSUE: 1 DOCUMENT TYPE: NEWSLETTER
PUBLISHER: PHILLIPS BUSINESS INFORMATION
LANGUAGE: ENGLISH WORD COUNT: 587 RECORD TYPE: FULLTEXT

COMPANY NAMES (DIALOG GENERATED): Source Technologies

TEXT:
...from the Mas-Hamilton Group, of Lexington,
Ky. The locking device is designed specifically to **address** automated teller machine (ATM) security issues through the combined use of lock hardware, system software...a terminal operator. The LinkPlus Interactive 2.1 transfers files between different computer systems, delivering **data** directly to trading partners and value-added networks. Transactions are batched into a file and automatically sent **asynchronously** . Costs were not disclosed. (SDM, 919/552-1100.)
...

1/K/55 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

04624013 Supplier Number: 61353404 (USE FORMAT 7 FOR FULLTEXT)
GUEST VIEWPOINT:A CRITICAL LOOK AT IA-64 -- Massive Resources, Massive ILP, But Can It Deliver?
Hopkins, Martin
Microprocessor Report, v14, n2, pNA
Feb, 2000
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 3580

... well as instructions to modify, test, and retrieve NaT values. Moving loads ahead of stores (**data** speculation) requires a memory-alias-detection table-in IA-64 this hardware table is called the advanced-load- **address** table, or ALAT. Special loads place entries in the ALAT, and stores whose **addresses** match an ALAT entry will remove that entry. For **data** speculation, check instructions access the ALAT to detect stores to a memory location that has been fetched by a load that was moved ahead of the store. (**Data** speculation can use a check load that does the recovery in some simple cases.) The...stack- frame overflow might occur at a frequent call point, a register stack engine (RSE) **asynchronously** saves and restores registers in the background. This RSE mechanism must take page faults, etc...

1/K/56 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

04487439 Supplier Number: 57588385 (USE FORMAT 7 FOR FULLTEXT)
PATENT WATCH. (News Briefs)
Belgard, Rich
Microprocessor Report, v13, n15, pNA
Nov 15, 1999
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 667

... processor.

The claims include a function unit that contains at least a function register, a **data** register, a result **address** register and a monitoring circuit. When the function, **data** and **address** registers have been loaded, as detected by the monitoring circuit, the function unit may begin its operation, **asynchronously** .

5,903,750

Dynamic branch prediction for branch instructions with multiple targets

Filed: November 20...

1/K/57 (Item 3 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
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03892961 Supplier Number: 50046600 (USE FORMAT 7 FOR FULLTEXT)
-IBM: Lotus to add real-time collaboration to LearningSpace
M2 Presswire, pN/A
June 3, 1998
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 1009

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...This will allow students to work at their own time and convenience on a course (**asynchronously**) and then, at a specific time and date, meet with their instructors and/or classmates...

...partnerships that make it easy for customers to rapidly deliver high-quality learning experiences. To **address** the need for ready-to-use content, Lotus is working with leading developers of corporate...already in use at corporations, colleges, and universities worldwide. *M2 COMMUNICATIONS DISCLAIMS ALL LIABILITY FOR **INFORMATION** PROVIDED WITHIN M2 PRESSWIRE. **DATA** SUPPLIED BY NAMED PARTY/PARTIES.*

1/K/58 (Item 4 from file: 636)
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03673434 Supplier Number: 47915837 (USE FORMAT 7 FOR FULLTEXT)
TIBCO BELIEVES PUSH-BASED MESSAGING WILL PULL BUSINESS AWAY FROM ITS RIVALS
Computergram International, n3227, pN/A
August 18, 1997
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 255

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...inefficient use of bandwidth, especially in high-volume applications environments such as Web servers and **data** warehouses. Tibco says TIB/Rendezvous pushes message to servers **asynchronously** and ensures each request is only handled once, by using a server-based scheduler to...

...respective Internetprotocol (IP) multicasting technologies to create a single specification for reliable multicasting - including subject **addressing** - they will submit for standardisation to the Internet Engineering Task Force some time next year...

1/K/59 (Item 5 from file: 636)
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03286591 Supplier Num[redacted]: 46749432 (USE FORMAT 7 FOR [redacted]LTEXT)
MESSAGE-ORIENTED MIDDLEWARE ASSOCIATION, COOL TO IBM's MQSERIES OFFER, IS STILL SEEKING COMMON MESSAGING GROUND
Computergram International, n3009, pN/A
Sept 30, 1996
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 482

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...by processes running on distributed systems. A process running on one system can instruct or **address** a process on another system over a network **asynchronously** , and unlike remote procedure calls, which literally invoke remote procedures onto the local system, transmits...

...a database management system or an operating system. In heterogeneous environments, clients have to exchange **information** across networks using multiple communications protocols and operating systems environments. Candle vice-president of solutions...

1/K/60 (Item 6 from file: 636)
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02775643 Supplier Number: 45632468 (USE FORMAT 7 FOR FULLTEXT)
MESSAGE-ORINETED MIDDLEWARE BODY IS "YEARS AWAY" FROM GOAL OF INTEROPERABLE MESSAGING MIDDLEWARE
Computergram International, n2693, pN/A
June 27, 1995
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 407

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...seeking a standard that will govern messaging software. Introducing its white paper, Building Your Enterprise **Information** Infrastructure With Message Oriented Middleware, the Association, which has stolen MOMA, the acronym by which...

...also director of strategic alliances at PeerLogic Inc, said this kind of problem will be **addressed** by the market over time and said the association's task is only to "educate...

...processes running on distributed systems. It enables a process on one system to instruct or **address** a process on another system over a network **asynchronously** , and - unlike remote procedure calls which invoke remote procedures onto the local system - transmits multiple...

...a database management system or an operating system. In heterogeneous environments clients have to exchange **information** with database servers across a network, using different communications protocols and operating systems. "MQSeries and message -oriented middleware in general is in the business of getting this **information** across," said Steve Craggs, business manager of IBM Corp's MQSeries messaging software based in...

1/K/61 (Item 7 from file: 636)
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02775642 Supplier Number: 45632467 (USE FORMAT 7 FOR FULLTEXT)
MESSAGE-ORIENTED MIDDLEWARE BODY IS "YEARS AWAY" FROM GOAL OF INTEROPERABLE MESSAGING MIDDLEWARE
Computergram International, n2693, pN/A

June 27, 1995
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 406

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...seeking a standard that will govern messaging software. Introducing its white paper, Building Your Enterprise **Information** Infrastructure With Message Oriented Middleware, the Association, which has stolen MOMA, the acronym by which...

...also director of strategic alliances at PeerLogic Inc, said this kind of problem will be **addressed** by the market over time and said the association's task is only to "educate...

...processes running on distributed systems. It enables a process on one system to instruct or **address** a process on another system over a network **asynchronously** , and - unlike remote procedure calls which invoke remote procedures onto the local system - transmits multiple...

...a database management system or an operating system. In heterogeneous environments clients have to exchange **information** with database servers across a network, using different communications protocols and operating systems. "MQSeries and message-oriented middleware in general is in the business of getting this **information** across," said Steve Craggs, business manager of IBM Corp's MQSeries messaging software based in...

1/K/62 (Item 8 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

02139096 Supplier Number: 43994677 (USE FORMAT 7 FOR FULLTEXT)
JAPAN's CHIP CONTENDERS FOR DIGITAL ASSISTANT MARKET - 2: HITACHI's FULL-FEATURED ENTRY
Computergram International, n2220, pN/A
July 28, 1993
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 1315

... chip solution. Both chips include a 32-bit RISC-based CPU and a 32-bit **address** bus. Although they hobble along on a 16-bit external bus, there is a 22-bit unmultiplexed **data** bus for designers that want to **address** up to 4Gb of RAM. The chips run at either 5V or 3.3V in...

...of them externally. Also included are two serial ports which can be programmed synchronously or **asynchronously** at baud rates decided by the chip's internal clock - up to 5M-bits per...

1/K/63 (Item 9 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

01124226 Supplier Number: 40860312 (USE FORMAT 7 FOR FULLTEXT)
An Industry First: Four-Port SRAMs From IDT
Semiconductor Industry & Business Survey, v11, n9, pN/A
July 10, 1989
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 219

... performance multiprocessing and DSP applications, including radar systems, LANs and graphics processors.
Featuring independent asynchronous **address** , **data** and control

lines, each port communi[redacted]es via a standard SRAM interfa[redacted]that can access any location in memory simultaneously and **asynchronously** . This feature enables multiple controllers or processors to simultaneously access the same memory space, resulting...
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              DDRESS?
S2          0   S1 AND COLLECT? (5N) (PAYMENT OR FEE)
S3          2   S1 AND (PAYMENT OR FEE)
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S1	63	(INFORMATION OR DATA OR DOCUMENT) (S) ASYNCHRONOUSLY (S) ADDRESS?
S2	0	S1 AND COLLECT? (5N) (PAYMENT OR FEE)
S3	2	S1 AND (PAYMENT OR FEE)
S4	1109	(COLLECT? OR PAY?) (5N) (INFORMATION OR DOCUMENT) (S) (EMAIL OR MAIL) (5N) ADDRESS?
S5	21	S4 AND (DETERMIN? OR COMPUT? OR CALCULAT?) (5N) (PAY? OR FEE)

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